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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/823,679	03/30/01	MAGOON R	050321-1880

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EXAMINER	
NGUYEN,H	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 11/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Offic Action Summary	Application No. 09/823,679	Applicant(s) MAGOON ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner. (post office Address Omitted)

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to because in figures 1, 2 and 4-16, the blank boxes representing the elements of the circuits have no labels. Applicant is required to label them with the symbols of each element or at least label them with formal functions. Correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "an inverter" of claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5 and 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 5, the recitation "an inverter" on line 1 is indefinite because it is unclear in what drawing the "an inverter" is read on.

Regarding claim 6, the recitation " a second terminal" on line 5 is indefinite because the connection is not complete i.e., the "a second terminal" is left dangling. The recitation "the control signal" on lines 10 and 13 is indefinite because it is unclear as to this "the control signal" is the same as or different than the "a control signal" on line 5. The control signals are labeled differently in the drawings and the specification does not disclose the relationship among these control signals.

Claims 7 and 8 are rendered indefinite by the deficiencies of claim 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102 (b) as being anticipated by Pace (US Pat. 5,204,562).

Regarding claims 1 and 2, figure 1 of Pace show s a transistor circuit for implementing a switch, comprising: a first switch node (14) configured to connect to an external circuit; a second switch node (16) configured to connect to the external circuit; a transistor device (12) having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal; a third switch node (18) for receiving the control signal; and a circuit (32) connected to the third switch node and the third terminal of the transistor device, the circuit having an impedance configured to reduce the parasitic capacitance of the transistor device (see col.2 lines 35-40). Transistor (12) is a MOSFET.

Claims 1 and 2 are rejected under 35 U.S.C. 102 (e) as being anticipated by Kuang et al. (6,281,737).

Regarding claims 1 and 2, figure 2 of Kuang show s a transistor circuit for implementing a switch, comprising: a first switch node configured to connect to an external circuit; a second switch node configured to connect to the external circuit; a transistor device (210) having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal; a third switch node for receiving the control signal; and a circuit (250, 260) connected to the third switch node and

the third terminal of the transistor device, the circuit having an impedance configured to reduce the parasitic capacitance of the transistor device. Transistor (210) is a MOSFET.

Claims 3 and 4 are rejected under 35 U.S.C. 102 (b) as being anticipated by Simmons et al. (5,223,751).

Regarding claims 3 and 4, figure 3 of Simmons shows a transistor circuit for implementing a switch, comprising: a first switch node configured to connect to an external circuit; a second switch node configured to connect to the external circuit; a transistor device (38) having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal (28) for controlling the electrical connectivity between the first terminal and the second terminal; and a circuit (36) connected to the second terminal of the transistor device, the circuit configured to provide a voltage (Vcc) to the second terminal when the control signal engages the transistor device. Element (38) is a MOSFET.

Claims 3-5 are rejected under 35 U.S.C. 102 (b) as being anticipated by Waggoner et al. (5,532,630).

Regarding claims 3-5 figure 4 of Waggoner shows a transistor circuit for implementing a switch, comprising: a MOSFET transistor device (8n), a circuit (8p and inverter 10n, 10p) connected to the second terminal of the transistor for providing a voltage to the second terminal when the gate of (8n) is activated. For instance, when the gate of (8n) is at high voltage, the drain of (8n) is at low voltage.

Allowable Subject Matter

Claims 6-8 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 6-8 would be allowable because the prior art of record fails to teach or fairly suggest a transistor circuit comprising: first transistor, second transistor and third transistors having their third terminals received a control signal; the third transistor having the first terminal

connected to the first terminal of the first transistor and the second terminal connected to the second terminal of the second transistor as called for in claim 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
Examiner
11-01-01

MY-TRANG NU TON
PRIMARY EXAMINER